Reply to Office Action dated: May 12.2010

Listing of the Claims:

52. (Currently Amended) A phased array for controlling a radiation pattern comprising:

an extended resonance circuit having an N plurality of ports; an antenna and a shunt impedance connected to each port;

the extended resonance circuit including a plurality of first tunable <u>series</u> impedances, one of which is connected between each of the N plurality of ports, each first impedance transforming the admittance of one port coupled to the first tunable impedance to the conjugate of the admittance for a serially adjacent second one of the N plurality of ports such that the voltage at each of the ports is the same magnitude across the circuit; and

a power source having an impedance matched to the impedance of an endmost port in the array.

- 53. (Previously Presented) The phased array of claim 52 wherein each of the first plurality of impedances is a tunable inductor.
- 54. (Previously Presented)) The phased array of the claim 53 wherein the series impedance between each port is a tunable transmission line, and the shunt impedance is a tunable capacitance.
- 55. (Currently Amended) The phased array of claim 52 wherein each of the plurality of first (series)impedances between each port includes two serially connected quarter-wave transformers with a tunable capacitor connected in shunt therebetween.
 - 56. (Previously Presented) The phased array of claim 52 further comprising: a single biased voltage to the endmost port in the array.
- 57. (Currently Amended) The phased array of claim 52, wherein the phase shift between successive ports is equal.

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- 58. (New) The phased array of claim 52 wherein each of the first impedances is a single series tunable impedance.
- 59. (New) The phased array of claim 52 wherein each of the shunt impedances connected to each port is a single tunable admittance.
- 60. (New) The phased array of claim 52 wherein each of the plurality of shunt impedances is identical for each port in the array and each of the plurality of first impedances is identical for each port in the array.